[stamp: Filed]

Priority Claim
[revenue stamp: 3,000 yen]
[revenue stamp canceled by illegible stamp]

Country of First Application

Application Date

Application Number

United States of America
July 6, 1970
No. 52637

[illegible stamp]

(21) Japanese Patent Application No.: S46-49495
(11) Unexamined Patent Application S47-2314
(43) Publication Date: February 4, 1972
Application for Inspection: Filed
(Total 6 Pages)

(19) Japan Patent Office
(13) Japanese Unexamined Patent Application Publication

Internal Filing Number

6151 53

(52) Japanese Classification

98(5)ED

[stamp: Suitable]
Request for Patent (1)
July [25], 1971
(2000 yen) [stamp: Suitable]

Patent Office Director General
Mr. Takehisa Ido

1. Title of the Invention
DEMODULATOR

2. Inventor
Name: Donald Walter Jantz
Address: 7 Stanley Drive
Framingham, Massachusetts
USA

3. Patent Applicant
Name: (757) RCA Corporation
Representative: M.S. Winters
Nationality: American
Residence: Rockefeller Plaza 30
New York, New York 10020
USA
[stamp: Japan Patent Office
July 6, 1971
Application 2nd Division
Yamazaki]

4. Patent Administrator Postal Number 651
Name (5376) Satoshi Kiyomizu
(and two others)
Address: c/o Kobe Newspaper Center
7-4 Kumoidoori, Fukiai-ku, Kobe
Tel: (078) 25-2211

46 049495 Formal Inspection (Ooi)
[illegible stamp]

Specifications

1. Title of the Invention

DEMODULATOR

2. Scope of Patent Claims

A demodulator that is equipped with (1) a peak detector that, in response to a sinusoidal wave, generates pulses with respect to each peak of a prescribed polarity of the sinusoidal wave; (2) an input terminal to which a compound signal consisting of a sinusoidal wave and another signal is applied; (3) an amplifier that has an output terminal that is connected to a charge storage medium; and (4) a switch that is connected between the output terminal of this amplifier and the charge storage medium; wherein said peak detector is operated such that it closes the switch in response to each pulse that is generated, and the demodulator is configured such that it charges said charge storage medium to the level of the amplified compound signal.

3. Detailed Description of the Invention

This invention is related to a demodulator circuit that uses a peak detector and a switch in order to generate signals that have not been specifically modulated (unmodulated signals) on the demodulator circuit.

In many of the presently known demodulators in this technical field, a transformer for the purpose of joining the reference carrier wave to the demodulator circuit is necessary. This is comparatively expensive, and it is furthermore inconvenient to install into an integrated circuit.

This invention can be implemented as a demodulator circuit consisting of a peak detector, a switch, and a charge storage medium.

The peak detector responds to an applied sinusoidal wave signal and generates one pulse for every peak of the given polarity of this waveform. A compound signal that consists of a sinusoidal wave signal and another signal is supplied to the input terminal of the amplifier. A switch is connected between the output terminal of this amplifier and the charge storage medium. This switch is closed in response to the pulses described above, and the charge storage medium is charged to the level of the signal that appears on the output terminal of the amplifier.

This invention is described in further detail below with reference to the drawings.

Peak detector 4, operational amplifier 6, switch 8, and charge storage medium – capacitor 10, for example – are included in peak demodulator 2, which is shown in Figure 1. A sinusoidal carrier wave that is not modulated is supplied to input terminal 12 of this detector 4.

[continued from previous page] For every peak that has a prescribed polarity in the carrier wave, one pulse is generated to output terminal 14 of the peak detector. For example, if the peak detector is to respond to negative peaks of the sinusoidal carrier wave, one pulse is generated to output terminal 14 for every negative peak of the carrier wave. Every time this sort of pulse is generated, switch 8 is closed only for the duration of the pulse, as shown by the dotted line that connects terminal 14 and switch 8.

A compound signal that contains a sinusoidal carrier wave, which has the same frequency as that described above but amplitude that has been modulated with an information signal, is applied to input terminal 16 of operational amplifier 6. Output terminal 20 of amplifier 6 is connected to terminal 18 of the switch. Every time switch 8 is closed, the signal on terminal 20 charges capacitor 10 through the switch. The electrical discharge circuit of the capacitor is formed by resistor 23, and that value is taken to be sufficiently large such that the discharge time constant of capacitor 10 is somewhat larger than the charge time constant. Accordingly, as explained in further detail below, a comparatively smooth voltage, in which the amplitude changes in step with changes within the signal modulated to the carrier signal, is generated between the terminals of capacitor 10.

The circuit described above is shown in further detail in Figure 2. Input terminal 12 of peak detector 4 is connected to one terminal of the charge storage medium – capacitor 26, for example – and capacitor 26 is connected to base electrode 28 of transistor 30 with the other terminal through current limiting resistor 32. Capacitor 26 is also connected to the ground of the circuit through resistor 34. Emitter electrode 36 is connected to the ground of the circuit through diode 38. Collector electrode 40 is connected to reference electric potential source -V1 through resistor 42, and it is connected to base electrode 46 of transistor 48 through union capacitor 50. Base electrode 46 is connected to reference electric potential source -V2, which is more negative than electric potential source -V1, through resistor 51. Emitter 52 is also connected to electric potential source -V2. Collector electrode 54 is connected to electric potential source -V1 through resistor 56, and it is connected to the emitter electrode of transistor 60 through resistor 52. Base electrode 64 of transistor 60 is directly connected to electric potential source -V1. Collector electrode 66 of transistor 60 is connected to output terminal 14 of peak detector 2, and it is connected to reference electric potential source +V1 through resistor 68.

Refer next to Figure 3, which shows several of the waveforms that appear within the circuit of Figure 2. Waveform A is an unmodulated sinusoidal carrier wave that is applied to input terminal 12 of peak detector 4. With the voltage drop from the diode effect between the base and emitter of transistor 30, as the portion that faces the negative side of waveform A reaches the threshold voltage (V_T) that is slightly more negative than the voltage to which the voltage drop in diode 38 is added, transistor 30 begins conduction. In Figure 3, conduction begins at time t_1 of waveform A, and capacitor 26 is charged. When transistor 30 reaches the conduction state, the negative voltage of that collector decreases and approaches the ground potential, as shown by waveform C. In step with the change of voltage applied to terminal 12, the conduction of transistor 30 is ended at time t_2 (waveform A) at which the connections of capacitor 26 with resistors 32 and 34 become more positive than the threshold voltage V_T. Accordingly, pulse 70 is formed on electrode 40 during the interval $t_1 - t_2$, and in the same way, it can be understood that a positive pulse (waveform C) is then formed with every negative peak that is generated following waveform A.

The positive pulse that is generated on collector electrode 40 is joined with the base electrode of transistor 48 through capacitor 50. Transistor 48 is driven by this pulse and begins conduction, and through this the negative pulse reaches terminal 14 through the emitter/collector pathway of transistor 60. As shown by D of Figure 3, a negative pulse is generated to output terminal 14 of the peak detector by each negative peak of the unmodulated sinusoidal carrier wave that is applied to input terminal 12.

Switch 8 of Figure 2 consists of two emitter transistors that have base electrodes 70 that are connected to output terminal 14. Collector electrode 72 is connected to the first emitter electrode 74 and output terminal 20 of operational amplifier 6. The second emitter electrode 76 forms terminal 22 of switch 8. Capacitor 10 and resistor 23 are connected in parallel between terminal 22 and the ground of the circuit.

High impedance (on the order of 250 megohms) is exhibited between terminal 20 and terminal 22 in the off-state due to the properties of the two-emitter transistor 8 that is used in this circuit. If this transistor reaches the on-state, impedance of approximately 50 ohms and a low offset voltage of approximately 50 microvolts between the first and second emitter electrodes 74 and 76 are exhibited. With a configuration such as that shown in the figure, in which the first emitter electrode 74 is directly connected to connector electrode 72, transistor 8 works as a bidirectional device. If a negative pulse is generated on terminal 14, transistor 8 enters the on-state. If a negative signal appears on terminal 20, current flows from the ground to the input terminal of operational amplifier 6 through capacitor 10, terminal 22, emitter 76 – emitter 74, terminal 20, and feedback resistor 80, and a negative waveform is generated between both of the terminals of the capacitor. Conversely, if a positive signal appears on terminal 20, current flows from terminal 20 to the circuit's ground through the relatively low impedance path of emitter 74 – emitter 76, and through capacitor 10, and the capacitor is pinched to form a positive waveform.

If the collector is relatively positive in the aforementioned case, current also flows from collector electrode 72 to terminal 14 of peak detector 2 through base electrode 70. The size of the collector–base current is larger than the emitter–emitter current. However, because of the high loop benefit of operational amplifier 6 (50 decibels higher), this size is not so large as to disrupt the waveform that appears on both ends of capacitor 10.

For switch 8, it is possible to use a standard bipolar transistor that has one emitter electrode. However, if this sort of transistor is used, the current will only flow in one direction, and a high offset voltage of approximately 30 millivolts will generate between the collector–emitter. Thereby, as a result of this, it will only be possible to demodulate signals of only one polarity having a high offset voltage. In contrast to this, through the two-emitter transistor, it becomes possible to demodulate signals that have a low offset voltage, having both positive and negative polarity.

Next, consider the case in which a demodulator signal such as that shown by waveform B in Figure 3 is applied to terminal 15. As previously stated, this demodulator signal B is a signal of the sinusoidal wave carrier wave with a frequency equal to that of waveform A, and is modulated by an information signal. This waveform B, which is generated by the modulator (not shown in the figure), is presumed to be in phase with waveform A. In the interval $t_1 - t_2$ (Figure 3), negative signal 80 (waveform B) is created on terminal 20 of amplifier 5. Coinciding with negative signal 80, negative pulse 72a (waveform D) is created on terminal 14 of peak detector 72. Through this, transistor 8 reaches the on-state. Thereby, current flows from the circuit's ground to terminal 20 through capacitor 10 and the low impedance path between emitter 76 – emitter 74. Capacitor 10 is charged until it becomes effectively equal to the negative level of the waveform on terminal 20. This is shown by 82 of waveform F (Figure 3). For every time interval in which transistor 8 is turned on, capacitor 10 is consecutively charged to the negative level of the signal that is generated on terminal 20.

The sum of the conduction impedance between the emitter – emitter and the output impedance of the operational amplifier is approximately 50 ohms. The capacitance of capacitor 10 is approximately 0.01 microfarads. Through this, the charging time constant becomes approximately 0.5 microseconds. Capacitor 10 is effectively charged to the level of the signal on terminal 20 with approximately 6.0 time constants. Accordingly, each pulse 72 (waveform D) that is applied to the control terminal of switch 8 must have a duration slightly longer than 3.0 microseconds. Resistor 23 has impedance of approximately 1 megohm, and through this a discharging time constant of approximately 10 milliseconds is provided. Thereby, as a result of this, if waveform A is presumed to be a waveform that has a period of 200 microseconds, capacitor 10 discharges very little between pulses. Thus, smooth waveform F that corresponds to a modulated envelope appears on both sides of capacitor 10.

Next, it is presumed that the phase of waveform B that is generated by the modulator (not shown in the figure) is shifted by exactly 180° from waveform A. For example, suppose that positive signal 84 (waveform B) is generated on terminal 20 of amplifier 6 during time period $t_3 - t_4$ (Figure 3). Coinciding

with the positive signal 84, negative pulse 72b (waveform D) is generated on terminal 14 of peak detector 72, [continued on next page]

[continued from previous page] and through this, transistor 8 reaches the on-state. Thereby, current flows from terminal 20 through emitters 74 and 76, and the capacitor 10 is effectively charged to the positive level of terminal 20. This is expressed by 86 of waveform F (Figure 3). For each successive time period in which transistor 8 is turned to the on-state, capacitor 10 is charged to the positive level of the signal that is generated on terminal 20. Once again, a modulated envelope appears on both sides of capacitor 10.

The full-wave peak demodulator that implements this invention is shown in Figure 4. This is similar in many respects to the peak demodulators of Figure 1 and Figure 2. In addition to these, an input terminal is attached to output terminal 20 of amplifier 6, and inverter 88 to which output terminal 90 is connected is established on the connection between the collector of the PNP-type two-emitter transistor 94 and the first emitter that comprise the second switch in the circuit. The second emitter 96 is connected to terminal 22. Base electrode 98 of transistor 94 is connected to the output terminal of positive peak detector 100, and detector 100 is equipped with an input terminal that is connected to terminal 12.

Every time a negative peak of the sinusoidal wave carrier wave that is applied to terminal 12 is detected, the circuit of Figure 4 operates in the same manner as the circuits of Figure 1 and Figure 2. When a positive peak is detected by device 100, a negative pulse is applied to base electrode 98 of device 94, this is turned on, and switch 8 is turned off. At the same time, the positive signal that appears on output terminal 20 of amplifier 6 is inverted by device 88, and capacitor 10 is charged to the level of the signal that appears on terminal 90. Accordingly, the full-wave peak demodulator operates with twice the information rate of the half-wave peak demodulators shown in Figure 1 and Figure 2. Through this, the envelope that appears on output terminal F is further smoothed.

Figure 5 shows a full-wave averaging demodulator, and this operates quite similarly to the demodulator of Figure 4. However, the second switch of this circuit is NPN-type two-emitter transistor 102, and its collector electrode and first emitter electrode are both connected to output terminal 90 of inverter 88. Its second emitter is connected to terminal 22. Base electrode 104 is the same as base electrode 70 of switch 8, and it is connected to the output terminal of rectangular wave generator 106.

Rectangular wave generator 106 generates rectangular waves with frequency f. The carrier wave signal with modulated amplitude that is applied to terminal 16 of amplifier 6 has the same frequency f. At each negative portion of the square wave, the circuit of Figure 5 operates in the same manner as each of the circuits of Figures 1, 2, and 4. At each positive portion of the square wave, NPN-type transistor 102 is turned on, switch 8 is turned off, and capacitor 10 is charged to the level of the signal at terminal 90.

4. Brief Description of the Drawings

Figure 1 is a diagram that generally shows the example of embodiment of this invention. Figure 2 is a diagram that shows in further detail the example of embodiment of this invention shown in Figure 1. Figure 3 is a diagram that shows one group of waveforms for the purpose of helping to understand the operation of the circuit of Figure 2. Figure 4 is a schematic circuit diagram of the full-wave demodulator that implemented this invention. Figure 5 is a schematic circuit diagram of the full-wave averaging demodulator that implemented this invention.

4...peak detector
6...amplifier
10...charge storage means
8...switch
16...terminal to which a compound signal is applied
12...input terminal to which an unmodulated sinusoidal wave is applied

Patent Applicant RCA Corporation
Agent Satoshi Kiyomizu (2 additional individuals)

[see source for figures]

Figure 1
Peak detector 4

Figure 4
Inverter 88
Negative peak detector 4
Positive peak detector 100

Figure 2

Figure 5
Rectangular wave generator 106

Patent Applicant RCA Corporation
Agent Satoshi Kiyomizu (2 additional individuals)

Figure 3

Patent Applicant RCA Corporation
Agent Satoshi Kiyomizu (2 additional individuals)

5. Catalog of Attached Documents

(1) Specifications	1 copy
(2) Drawings	1 copy
(3) Power of Attorney and its Translation	1 copy of each
(4) Certificate of Priority Rights and its Translation	1 copy of each
(5) Copy of Application	1 copy
(6) Request for Examination of Application	1 copy
(7) Written Statement	1 copy

6. Additional Agents

Name ([8299]) Hiroshi Tanaka
Address: 7-4 Kumoidoori, Fukiai-ku, Kobe
Kobe Shimbun Kaikan [Kobe Newspaper Center]
Tel: (078) 25-2211

Name ([6229]) Masa[aki] Shouji
Address: Same as above